A 1.8V 10-BIT 100MS/S FULLY DIFFERENTIAL PIPELINED ADC IN CMOS 0.18uM PROCESS TECHNOLOGY

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BY

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

MS/s	Mega sample per second
ADC	Analog to digital converter
mW	miliwatt
CMRR	Common Mode rejection ratio
CEDEC	Collaborative Microelectronics Design Excellence Centre
TGATE	Thick gate
FVF	Flipped Voltage Follower
MDAC	Multiplying digital to analog converter
IEEE	Institute of Electrical and Electronics
SoC	System On Chip
DEC	Digital Error Correction
MUX	Multiplexer
SFDR	Spurious Free Dynamic Range
MOM	Metal On Metal
Op Amp	Operational Amplifier
PMOS	P type transistor
NMOS	B type transistor
GBW	Gain bandwidth
CMFB	Common Mode Feedback
Ph1	Phase 1 clock
Ph2	Phase 2 clock

PEREKAAN ADC BERSALURAN PAIP DENGAN KUASA PENSAMPELAN 100MS/s, PENGUNAAN KUASA 1.8V, MASUKAN BERCIRI PEMBEZAAN DAN PROSES TEKNOLOGI 0.18UM

ABSTRAK

Piawai Bluetooth™ merupakan salah satu penggerak utama bagi perhubungan tanpa wayar berjarak pendek. Kandungan Piawai Bluetooth™ adalah dari frekuensi 500Khz ke 25Mhz. Untuk pensampelan frekuensi serendah 3 Mhz ke bawah, rekaan ADC berciri SAR dan Delta-Sigma adalah pilihan utama manakala rekaan ADC berciri saluran paip adalah lebih sesuai untuk pensampelan frekuensi 5 MHz ke atas Matlamat penyelidkan ini adalah untuk memghasilkan rekaan ADC berciri saluran paip yang boleh digunakan untuk piawai Bluetooth™ dari BT1.1 sehingga BT4.0 dengan kuasa pensampelan sehingga 100MS/s dan 10 bit resolusi dengan bekalan kuasa 1.8V di bawah proses teknologi CMOS 0.18um dari Silterra. Operasi penguat berciri Flipped Voltage Follower (FVF) telah disyorkan untuk mencapai kuasa pensampelan yang tinggi. Rekaan ADC berciri saluran paip yang mengandungi 10 paip telah direka dan diuji di bawah pensampelan 50MS/s and 100MS/s. Pensampelan setinggi 50MS/s telah dicapai dengan penggunaan kuasa serendah 54mW. Peningkatan kuasa pensampelan boleh dicapai jika kuasa lebar jalur penguat di pertingkatkan melalui ciri penentukuran digital and litar suapbalik mod biasa.

A 1.8V 10-Bit 100MS/S FULLY DIFFERENTIAL PIPELINED ADC IN CMOS 0.18UM PROCESS

ABSTRACT

The Bluetooth™ standards is one of the major driving forces of the short-range wireless communications market as well as home and office environments. There are many Bluetooth™ standards covering the signal bandwidth from 500 KHz to 25 MHz. For low frequency data sampling, SAR and Delta-Sigma ADC are preferred architecture for signal bandwidth of below 3 MHz and pipelined ADC is prefer for 5 MHz and above. This research is to deploy pipelined ADC as single architecture that able to cover Bluetooth™ standard from BT1.1 to BT4.0. The targeted sampling rate is 100MS/s with 10 bit resolution at 1.8V power and designed using Silterra CMOS 0.18um process. Flipped Voltage Follower (FVF) operational amplifier has been recommended as operational amplifier to achieve high sampling rate .Ten stages pipelined ADC was developed and tested at 50MS/s and 100MS/s. The sampling rate has achieved by measureable of 50MS/s and the power consumption is 54mW. Sampling rate can be increased further by improving the gain bandwidth of the FVF Op-Amp through the implementation of the digital calibration and common mode feedback (CMFB) circuit.

CHAPTER 1

INTRODUCTION

1.1 Background

Analog to Digital Converter (ADC) is an essential component in modern world electronic devices such as cellphone, digital camera, and microphone. It converts the analog signal into digital domain for post processing by microcontroller. This will allow us to use electronic devices to interact with the analog world through complex sensory technologies. Besides, for sensory technology, ADC is widely used as component of wireless communication such as WIFI and Bluetooth interface. There are few types of ADC architecture like Successive Approximation, Sigma Delta, Flash and Pipeline ADC. The usage of the each ADC type is depended on the specification of the product in term of sampling rate, resolution, power consumption and the cost of the silicon die. There are four different segments of usage of ADC, which are data acquisition, precision industrial measurement, voice band and audio and high-speed communication (Walt Kester et al.,2005). For the lower speed segment like voice band audio, precision industrial that focus more on data accuracy, usually it is filled by the sigma delta architecture. For medium speed around 10KS/S to 100KS/S, it is filled by the Successive Approximation architecture. For speed higher that 100MS/s and above, Flash ADC is popular. For speed from 5MS/S and above, pipelined ADC is the preferred architecture. Each of the architecture has its own feature for example the Flash ADC has advantage of speed but it has to double its size for each bit added, this will increase input capacitance and consumes more power.

The pipeline ADC has the number of stages increases only with the numbers of bits and speed is higher but it has high latency. The Successive Approximation architecture uses only one comparator and lower power consumption but the size will grow with the number of bits and it takes many cycles to converge to the final result. The Sigma Delta architecture uses oversampling method and easier to design but only for low speed application such as audio sampling.

1.2 Problem Statements

The Bluetooth standards is one of the major driving forces of the short-range wireless communications market as well as home and office environments. It is deploying a carrier band at 2.4 GHz (Bo Xia et al.,2006). The summary of the specification for Bluetooth is as shown below

Table 1.1 Bluetooth Standards

Specification	BT1.1	BT1.2	BT2.0+EDR	BT2.1+EDR	BT3.0+HS	BT4.0
Adopted year	2002	2004	2005	2007	2009	2010
Transmission rate	723.1 kbps	723.1 kbps	2.1 Mbps	3Mbps	24 Mbps	25 Mbps
Standard range	10m	10m	10m	10m	10m	50m

Each standard will have different transmission rate varying from 723.1Kbps to 25Mbps. Notice that the data rate have increased from 3Mbps to 24Mbps from standard BT2.1 to standard BT3.0.

Table 1.2 below indicates the related works which have demonstrated the architectures recommended for Bluetooth standards above. For standard BT1.1 to BT2.1, preferred ADC architecture are Successive Approximation and Delta-Sigma modulation due to low sampling rate requirement. For BT standard 3.0 and above, pipelined ADC is preferred and usually it is shared with the WLAN application. Low power consumption and high sampling rate are two main factors that determine the architecture of the ADC. High sampling rate and resolution will lead to high power consumption while low power consumption will limit the choices of the sampling methodology.

Table 1.2 Related works on ADC architecture for Bluetooth Standards

Reference	Architecture	Signal BW	Sampling rate	Process	Device	VDD (V)	Watt
J. Grilo et al., 2001	Delta–sigma modulator	500Khz	32Mhz	0.35um	BICMOS	2.7	12mW
Junya Kudoh et al., 2001	Pipelined ADC	500Khz	13MS/S	0.35um	CMOS	2.8	8.9mW
K. Philips 2003	Delta–sigma modulator	500khz	64Mhz	0.18um	CMOS	1.8	4.4mW
Bo Xia et al., 2006	Pipelined ADC	11Mb/s	11Mhz/ 44Mhz	0.25um	BICMOS	2.5	12mW/ 20mW
Lilan Yu et al., 2016	SAR	500Khz	2MS/20MS	0.28nm	CMOS	1	0.94u/ 15.87u
E. Siragusa et al ., 2004	Pipelined ADC	500khz	40MS/s	0.18um	CMOS	1.8	400mW
B. J. Farahani et al., 2004	Delta–sigma modulator	1.5Mhz	45Mhz	0.18um	CMOS	1.8	5mW
Jinseok Koh et al ., 2004	Delta–sigma modulator	500Khz	37.5Mhz	0.13um	CMOS	1.5	1.65m W
Wilmar Carvajal et al., 2012	Pipelined ADC	500khz	11MS/s	0.35um	CMOS	3.3	12mW

.

Paper by (Bo Xia., 2006) in Table 1.2 has proposed a dual mode configuration which deploying separate architectures for each speed but that will increase the die size. The best option is to have a single architecture approach is essential in order to cover all Bluetooth standards.

Table 1.3 indicates the related works on the pipelined ADC architectures recommended which is able to fulfill the before mentioned standards. Research papers below only demonstrated the front end of the pipelined ADC without the digital error correction. The actual power consumption could be 20% higher than reported in the paper. At 0.18um process with power supply at 1.8V, most of the designed are 100mW at 100MS/s condition. It is desirable to have a pipelined ADC structure with digital error correction block included that able to achieve sampling rate of up to 100MS/s with power supply of less than 100mW at 1.8V power supply.

Table 1.3 Related works on pipelined ADC architecture

Title	Signal BW	Sampling rate	Process Tech	Device	VDD (V)	Current	Bit
Teng Chen et al,.2015	17Mhz	40MS/s	0.18um	CMOS	3.3	30mA	14
Zhenyu Wang et al., 2013	15.5 Mhz	100Ms/s	0.18uM	CMOS	1.8	51mA	14
Long Yang et al.,2013	5Mhz	100MS/s	0.18um	CMOS	1.8	116mA	16
Lei Luo et al., 2009	< 50Mhz	100MS/s	0.18um	CMOS	1.8	122mA	14
Yang Long et al., 2016	< 50Mhz	100MS/s	0.18	CMOS	1.8	34mA	16
E. Siragusa et al., 2004	500khz	40MS/s	0.18um	CMOS	1.8	222mA	15

This research is to deploy pipelined ADC as single architecture that able to cover standard from BT1.1 to BT4.0 with low power consumption. The architecture will propose Flipped Voltage Follower (FVF) as operational transconductance amplifier (OTA) to achieve high sampling rate and operating voltage at 1.8V.

1.3 Objectives

To design a 10 bit pipelined ADC with a minimum sampling rate of 50 MS/s and up to 100 MS/s, which cover the BT standard range of 723.1kbps to 25Mbps with power consumption less than 100 mV at power supply of 1.8V.

1.4 **Scope**

The research will be covering the design of the Flipped Voltage Follower (FVF) OTA based amplifier for pipelined ADC which operates at 1.8V, 10 bits resolution and sample rate up to 100MS/s. High sampling rate and low power consumption will be the main focus in this project. The simulation tool to be used is LTspice for circuit modelling and Cadence Virtuoso simulator to run analog simulation using Silterra 0.18um process library. Validation is mainly focused on MDAC block functionality and not full pipelined ADC level due to high complexity of the digital calibration and data error correction. Building block of Digital Error Correction will be partially work and data is needed for power estimation and future improvement only.

1.6 Thesis Outline

The remainder of this thesis consists of four chapters. The Literature Review in Chapter 2 is covering two parts. Part 1 covers basic building block of the pipelined ADC like MDAC, comparator, decoder, operational amplifier and digital error correction logic. Part 2 will cover the techniques that used by researcher to achieve high sampling rate and power consumption.

Chapter 3 describes the overall methodology of the research. It describes in detail the steps taken to construct the final pipelined ADC structure, how it works and how characterization work been carried out. Part 1 describes how the MDAC was modelled using the LTspice software and part 2 describes the circuit construction of the building including the FVF-OTA, comparator , decoder, multiplexer, digital error correction logic. Part 3 describes that characterization of the full model and the way to investigate the power consumption and accuracy

Chapter 4 contains the results of the simulation supported by explanations on their functionality and accuracy. Part one covers the result from the LTspice modeling on MDAC structure. Part two covers the simulation result of the circuit implementation in Cadence tool with Silterra 0.18μm process.

Chapter 5 wraps up this research with a conclusion, proposed several future works that useful to further improve the accuracy, speed and power consumption of the pipelined ADC.

CHAPTER 2

Literature review

2.1 Introduction

This chapter will outline the basic architecture of the pipelined ADC and the sub blocks of the ADC. Each of the sub block will be discussed on their usage and function. In addition, research work that contributed by researchers in this topic shall be reviewed especially on the innovation ideas that overcoming the design challenge to achieve better power consumption and high sampling goal.

The world is more "connected" these day and human interaction are more in advanced way. It has directly stimulated the growth of new IOT devices which increasingly the demand of ADC as an important component for SoC product. Analog sensor is needed to collect environmental raw data and transmit wireless channel to the server for post processing. Bluetooth interface has been used widely as transmission medium between the device and processor. Low power consumption is the most important requirement for Bluetooth devices which run on battery power.

2.2 ADC architecture overview

ADC applications can be classified into four broad market segments which are

1. Data acquisition which process of sampling the signals that measure the real world physical condition and converting into digital numeric value which can be post processed by a computer.
2. Precision industrial measurement which provide a simultaneous-sampling measurement system for signal acquisition applications such as power metering,

defibrillators and ECG monitors, as well as pressure sensors, coriolis flow meters and vibration/modal

3. Voiceband and audio which widely used in the music instruments and telecommunication.
4. High speed which sampling rate is more than 5MS/s like video camera and IF wireless transceiver.

Depending on the cost of the component, power requirement and accuracy of the data, there are several architectures that have been developed to support the application above.

1. Successive Approximation (SAR) for data acquisition

    - The input sample-and-hold (S/H) is to keep the signal constant during the conversion cycle. The conversion starts with the internal DAC converter (DAC) set to midscale. The comparator determines whether the S/H output is greater or less than the DAC output, and the result (the most-significant bit (MSB) of the conversion) is stored in the successive-approximation register (SAR) as a 1 or a 0. The DAC is then set either to 1⁄4 scale or 3⁄4 scale (depending on the value of the MSB), and the comparator makes the decision for the second bit of the conversion. The result (1 or 0) is stored in the register, and the process continues until all of the bit values have been determined. At the end of the conversion process, a logic signal End of conversion is asserted. The basic block diagram is shown in Figure 2.1 below

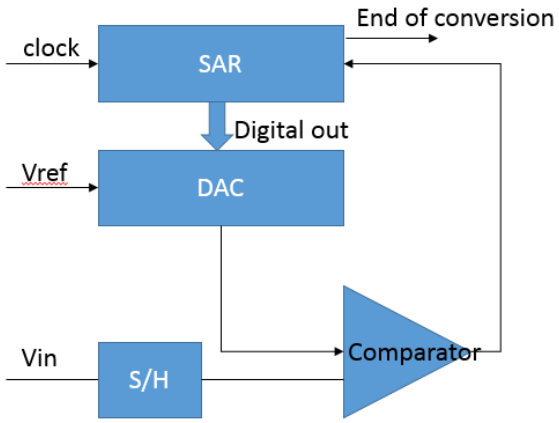

Figure 2.1 Successive Approximation (SAR) ADC

2. Sigma Delta ADC

- Figure 2.2 showing the structure of the sigma Delta ADC. The heart of this basic modulator is a 1-bit ADC (comparator) and a 1-bit DAC (switch). The output of the modulator is a 1-bit stream of data. Because of negative feedback around the integrator, the average value of the signal at point B must equal VIN. If VIN is zero (i.e., midscale), there are an equal number of 1s and 0s in the output data stream. As the input signal goes more positive, the number of 1s increases, and the number of 0s decreases. Likewise, as the input signal goes more negative, the number of 1s decreases, and the number of 0s increases. The ratio of the 1s in the output stream to the total number of samples in the same interval—the ones density—must therefore be proportional to the dc value of the input.

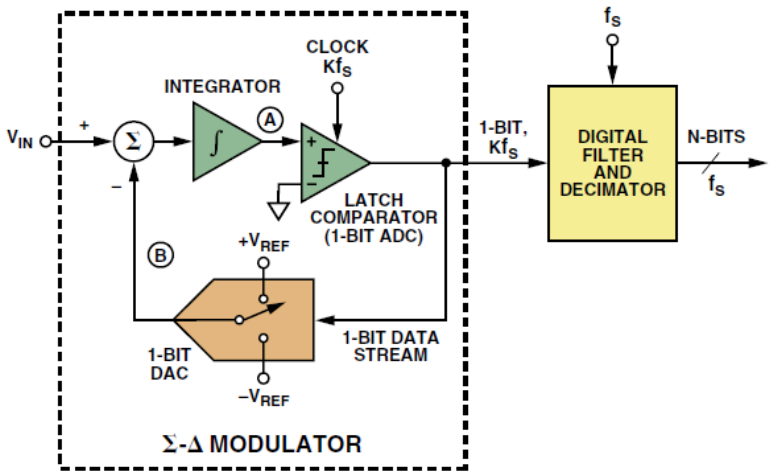

Figure 2.2 Sigma Delta ADC (Walt Kester et al.,2005).

3. Pipelined ADC.

- The pipelined ADC is the most popular architecture due to its advantage on the speed, power and accuracy. It is able to support operating range from 5MS/S up to 1GS/S. It can support many types of instrumentation applications (digital oscilloscopes, spectrum analyzers, and medical imaging). Also requiring high- speed converters are video, radar, communications (IF sampling, software radio, base stations, set-top boxes, etc.), and consumer electronics (digital cameras, display electronics, DVD, enhanced-definition TV, and high-definition TV). The detail of the pipelined ADC will be discussed in the next section.

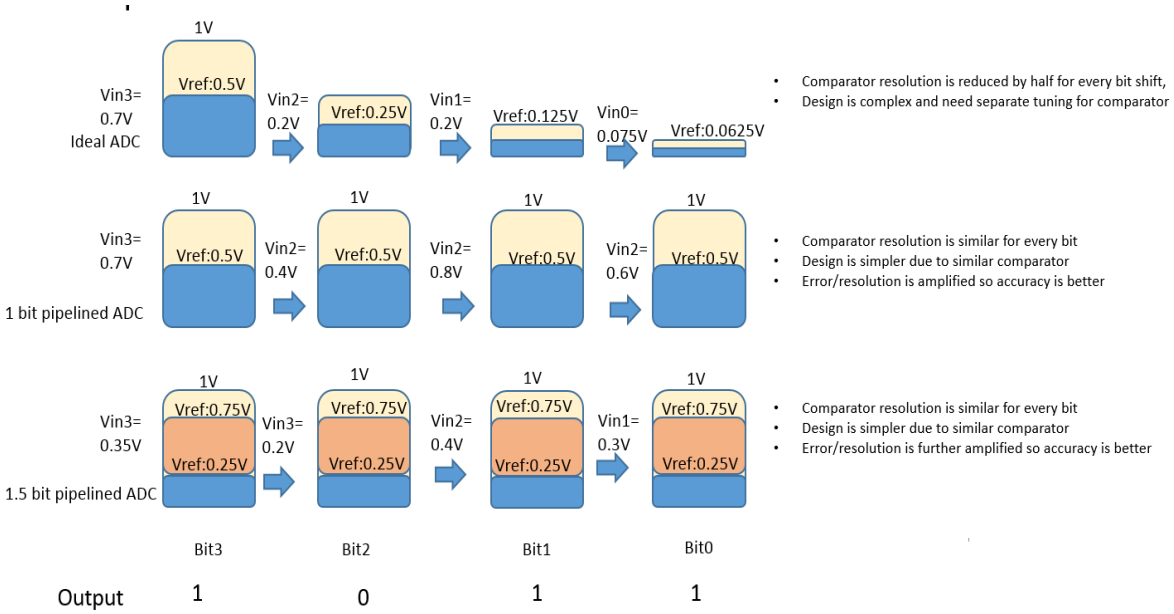

Figure 2.3 Basic pipelined ADC overview

Figure 2.4 below showing the types of ADC and their usage model

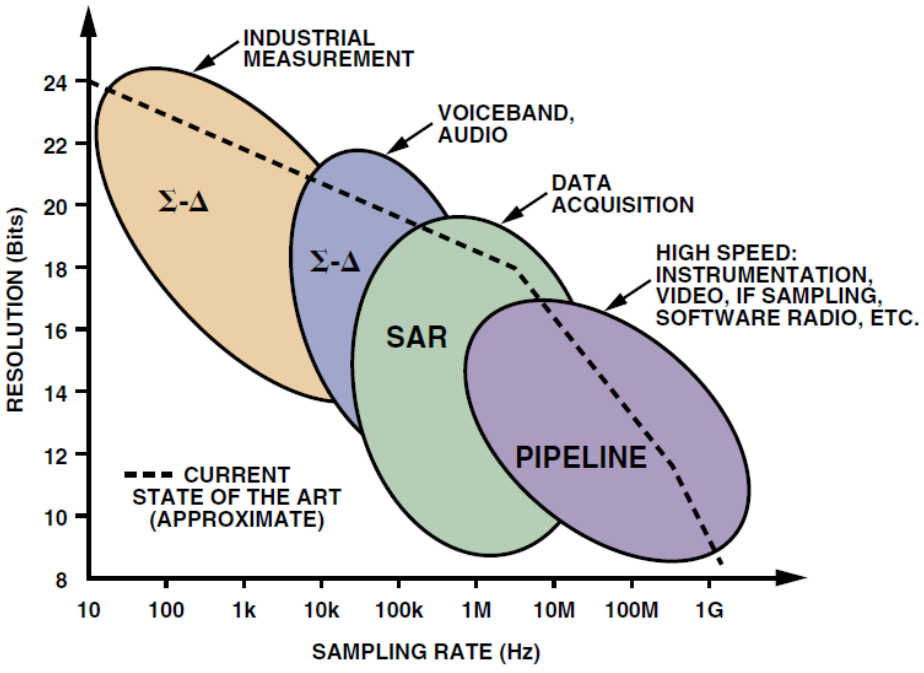

Figure 2.4 ADC sampling rate and usage model (Walt Kester et al.,2005).

2.3 Basic architecture of pipelined ADC.

Before moving to analyzing the contributions of the research committees, it is essential to understand the basic architecture of the pipelined ADC, Figure 2.5 below showing the basic architecture diagram (Teng Chen; Leli Peng et al., 2015)

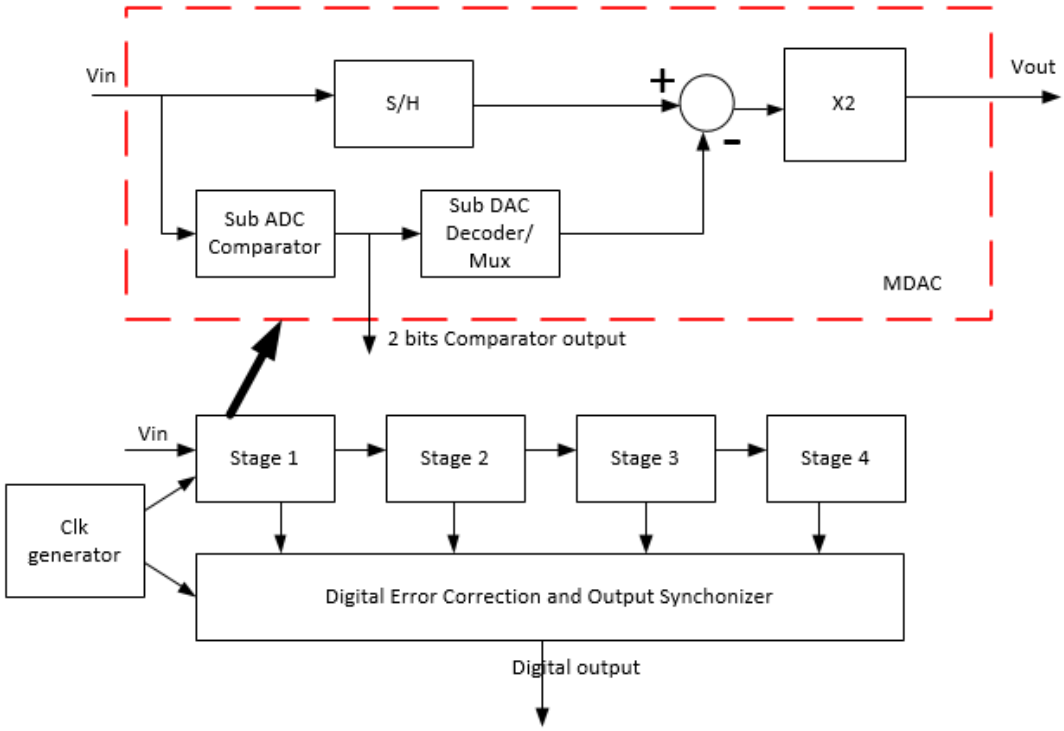

Figure 2.5 Pipelined ADC high level diagram

From the diagram of Figure 2.5 above, it is showing that the pipelined ADC is comprising of 3 major components which are the clock generator, 1.5 bits MDAC (Multiplying Digital to Analog Converter) and the DEC (Digital Error Correction) and putput synchronizer. The purpose of the clock generator is to generate the non-overlapping clock to the ADC system. The 1.5bits MDAC will perform sample and hold function and also generates 2 bits digital code to the digital error correction block for post processing. It will also generate residue output and pass to next stage of MDAC. The DEC will post process the digital output from MDAC and generate final digital output

that representing the magnitude of the analog signal. Here are the steps to descript how the system convert the analog signal to digital output

1. First the analog input is sampled by the sample/hold circuit in the MDAC block.
2. The same input signal is quantized by MDAC into 2 bits digital output by comparator. The digital code will be decoded in Sub-DAC of MDAC to determine the landing zone of the input signal
3. The sub DAC will generate a DC signal that to be subtracted by the input signal and late buffer out to the next stage by the OTA.

If the input is differential signal, the mathematic expression of the MDAC is (R. Jacob Baker.,2010)

$$Voutp = 2(Vinp + \overline{XY}\left(\frac{Vcm}{2}\right) - \bar{X}Y\left(\frac{Vcm}{2}\right) - XY\left(\frac{3Vcm}{2}\right) \quad (2.1)$$

$$Voutn = 2(Vinn + XY\left(\frac{Vcm}{2}\right) - \bar{X}Y\left(\frac{Vcm}{2}\right) - \overline{XY}\left(\frac{3Vcm}{2}\right) \quad (2.2)$$

Where *XY* are the 2 bits digital output from the comparator and it represents the landing zone which the input signal falling at. If Vmin and Vmax is minimum and maximum swing of the input signal, then VCM is the common mode voltage which equal to

$$Vcm = \left(\frac{Vmax - Vmin}{2}\right) \quad (2.3)$$

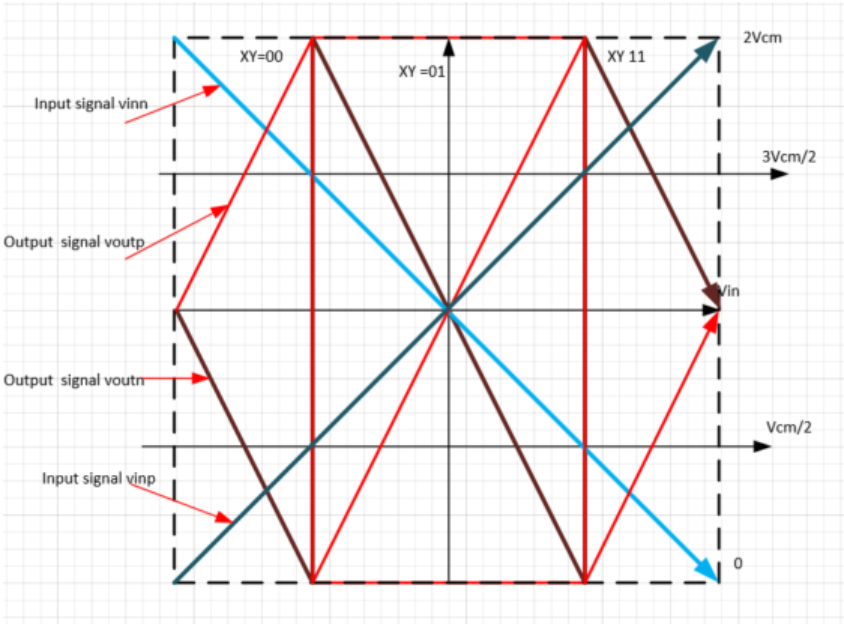

Figure 2.6 Pieplined ADC transfer curve

2.3.1 Clock generator

The function of clock generator is to generate 2 phase non- overlapping clock to carry out sample and hold operation and digital error correction function. The reason for using non-overlapping clock is to avoid charge feedthrough in the switched capacitor when switching between sample to hold phase. Usually The output clock is generated from the single source from PLL (phase lock loop) circuit and branching to Ph1 and Ph2 through the combinational logic connection, example of the clock generator is as Figure 2.7 below

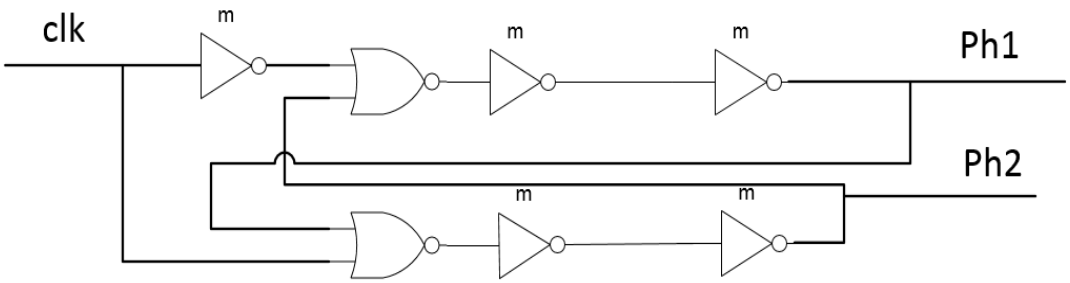

Figure 2.7 Basic clock generator

The non-overlapping clock will need to meet low jitter and precise duty cycle requirements. Low jitter means low cycle to cycle variations. If cycle to cycle jitter is high, system will encounter sampling error especially for high frequency input. As the clock is shared across MDAC stages the duty cycle variation will propagate sample and hold error to next stage. Figure 2.8a, Figure 2.8b and Figure 2.8c below showing how the non-overlapping clock looks like and how the clock jitter impacting the performance.

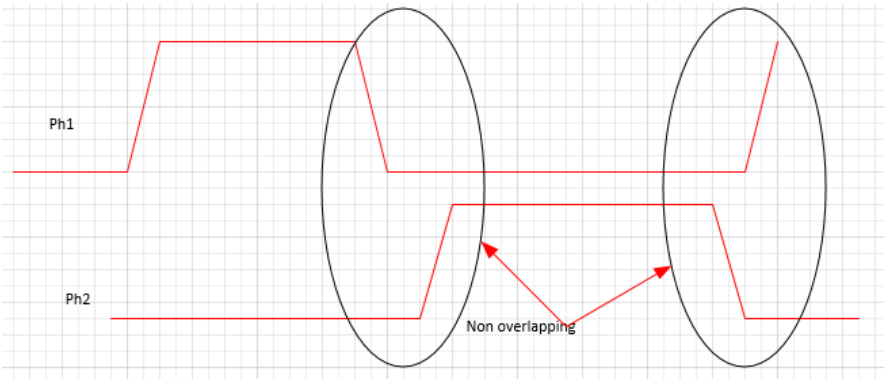

Figure 2.8a Ideal non-overlapping clock I

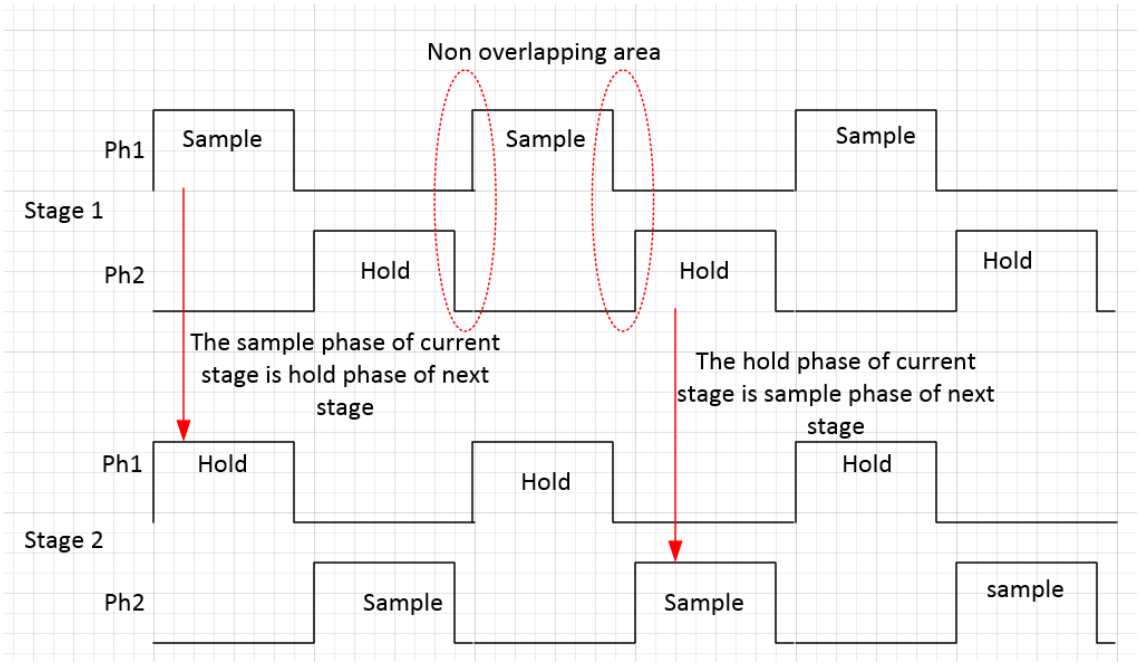

Figure 2.8b Ideal non-overlapping clock II

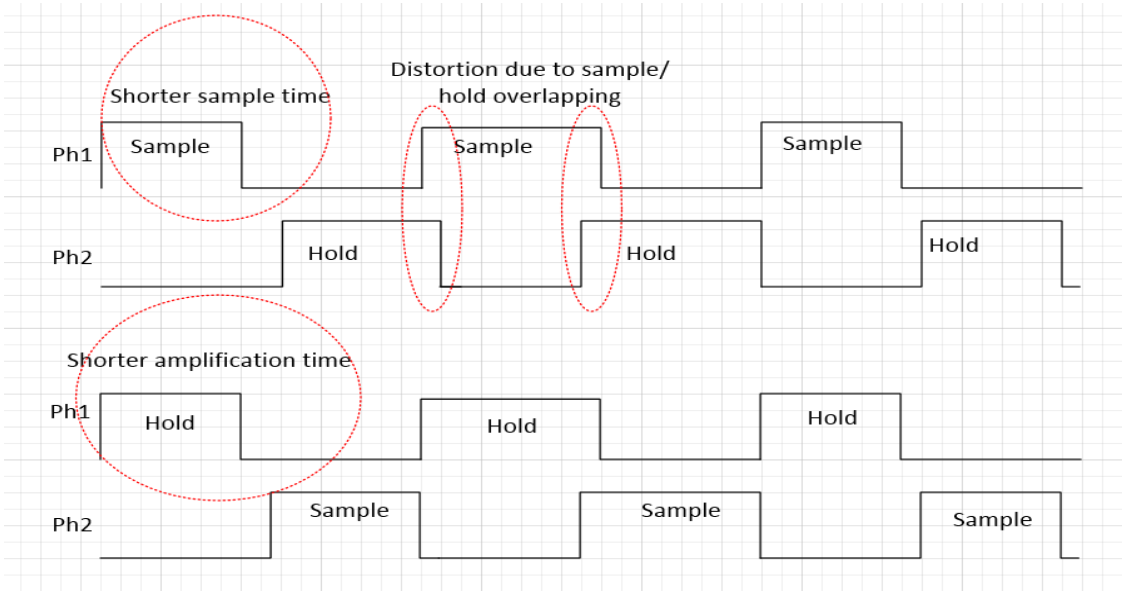

Figure 2.8c Ideal non-overlapping clock with error

If the sample clock is overlapping with hold clock, the previous captured analog level will be lost. On top of that, since the current sample clock is also be used as clock for hold phase. A shorter high time at current sample phase meaning a shorter hold period for the next stage. Besides, duty cycle variation will change the non-overlapping time. If the non-overlapping zone become smaller, sampling noise will be coupled into hold period, on the other hand, if the non-overlapping period is larger, it will impact the sampling or hold time. Inconsistent sampling period will impact non linearity performance (INL and DNL) while inconsistent hold period will impact settling level of the residue amplifier. One way to fix the clock jitter problem is to implement the DLL circuit to track the delay between the Ph1 and Ph2 through periodic adjustment. (R. Jacob Baker.,2010)

2.3.2 Multiplying Digital to Analog Converter (MDAC)

The function of the MDAC is to sample the input signal, compare against reference voltage to determine its landing zone, subtract with a predefined DC voltage and pass the residue output to the next stage to carry out similar operation. The residue output is the "error" or "remain" generated by MDAC. Figure 2.8 showing the basic block diagram of MDAC. Basically it is doing "coarse band" sampling to determine the location of the signal level landing at and passing the error residue to the next stage for fine band sampling

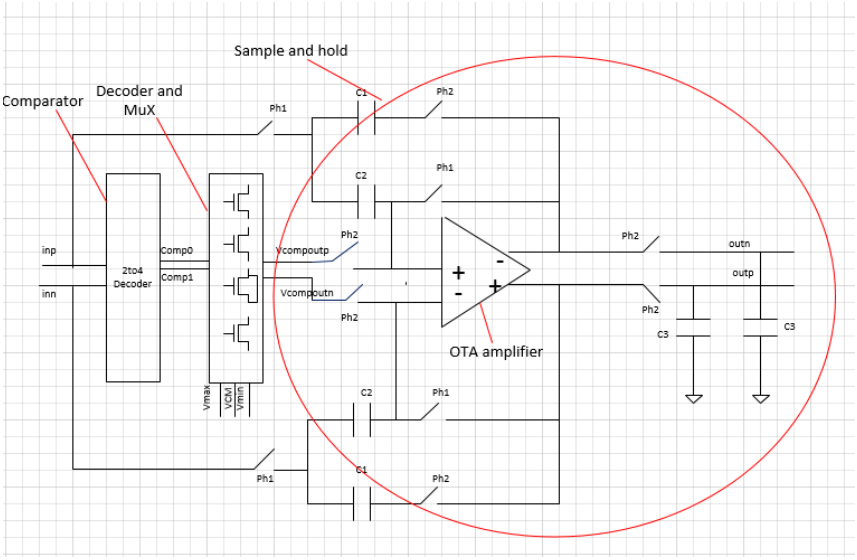

Figure 2.9 Building block of MDAC

Here are the steps to descript how the MDAC works

1. The MDAC compares the input signal against the reference voltage through the comparator. The comparator will generate digital output to the decoder.
2. The decoder will decode the 2 bits digital output from comparator and generates select signal to select the analog voltage output to the amplifier
3. Clock Ph1 will be high during sample time, the switch will turn **ON** and input signal will be sampled to C1 and C2. The op amp will be at unity gain stage, the output will follow the input voltage level. The input of differential amplifier will be set to VCM level
4. Clock Ph2 will be high during the hold period, this is the time when MDAC will perform the amplification and subtraction operation. The capacitor C1 and C2 will be connected in series hence it will perform the multiplication by 2 operation. Since the capacitor is connected to the output of the MUX, hence it will subtract the voltage from the MUX output. The result is the residue of

the operation and it will be hold at the capacitor C3 for next stage sampling.This steps are better illustrated in Figure 2.10 below

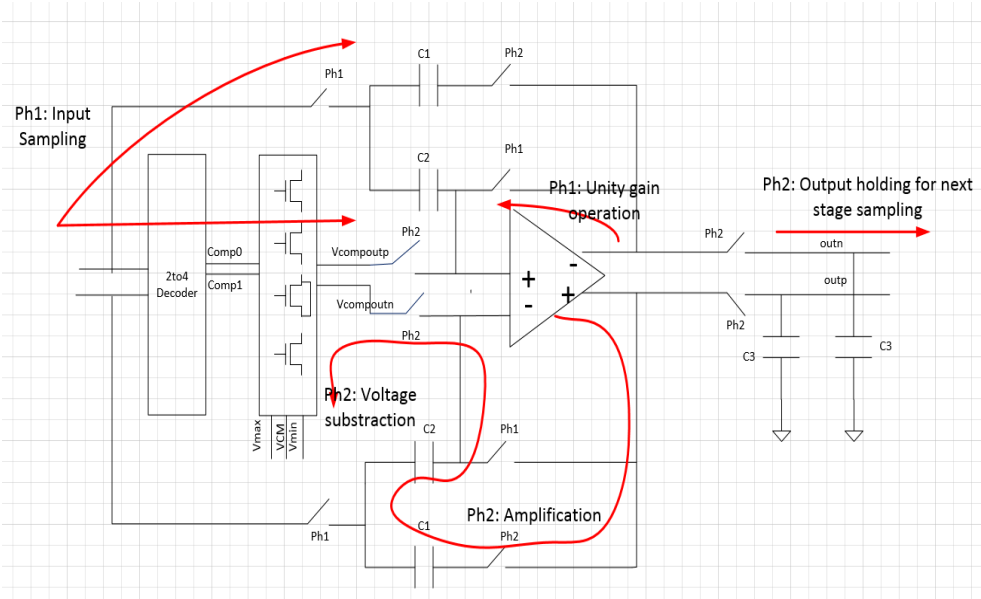

Figure 2.10 Sample and hold operation

2.3.2.1 Switched capacitor network for Sample and hold circuit

It is important component of pipelined ADC especially for IF application where wideband input signal requires high SFDR . Usually it is formed by a switched capacitor circuit and controlled by Ph1 and Ph2 clock. One of the disadvantages of the switch capacitor is when the output voltage of the switch is closer to the input voltage, the VGS of the switch transistor is large and the Vds is small. If Vds is far less than the overdrive voltage, the switch operates in the deep triode. This will slow down the speed of the sampling, basically the resistance of the switch is not linear across the Vds sweep [5]. On resistance is needed to be as small as possible, we could increase the W/L but it will introduce clock feedthrough noise(Ahmed M. A. Ali.,2010).

There are 2 factors that impacting the performance of switched capacitor circuit.

1. Signal dependent parasitic capacitance from input to AC ground during the sample phase (Cp) as shown in Figure 2.11 below. Causing non linearity charging current which travelled through its source resistance and it is larger at high frequency (Arsen Hekimyan et al., 2015).

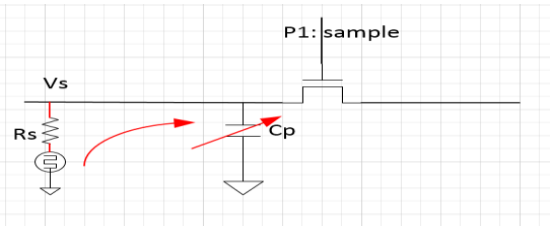

Figure 2.11 Signal dependent parasitic capacitance

2. Second factor is due to parasitic capacitance from input to the output during hold phase (Arsen Hekimyan et al., 2015). CP2 which can introduce feed forward disturbance to the output signal. During the hold phase, where the output of the switch is holding the previous sampled signal for output evaluation, the signal is still changing and will couple through transistor switch to output signal. This will distort the output signal. One way to neutralize the effect is to use a dummy capacitance CP3 to connect to the complementary input just like connection in Figure 2.13. It can be a transistor but this will add in junction capacitance to input or MOM capacitor and this will need to be carefully match.

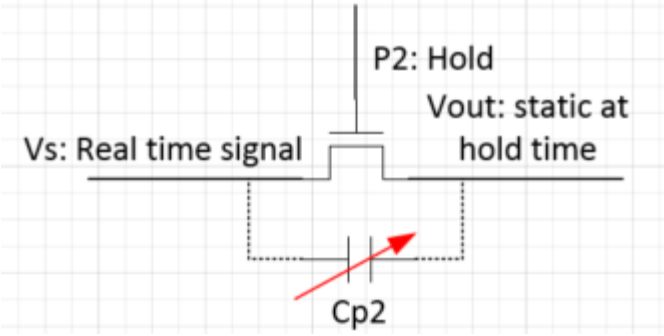

Figure 2.12 Parasitic capacitance

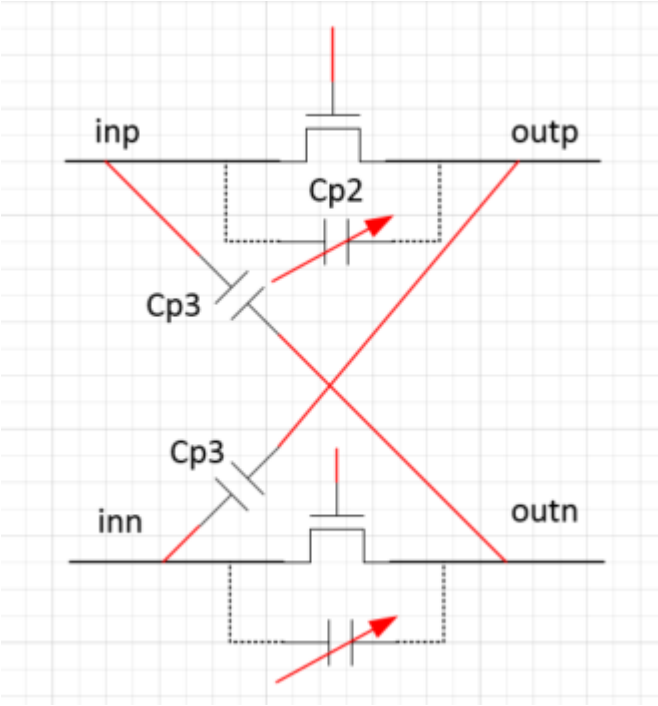

Figure 2.13 Method to improve junction capacitance

2.3.2.2 Comparator

The purpose of the comparator is to compare the differential input signal against the Vref signal to determine the zone of the differential input signal is falling at. Figure 2.14 below showing the diagram on how the zone of the differential signal been divided.

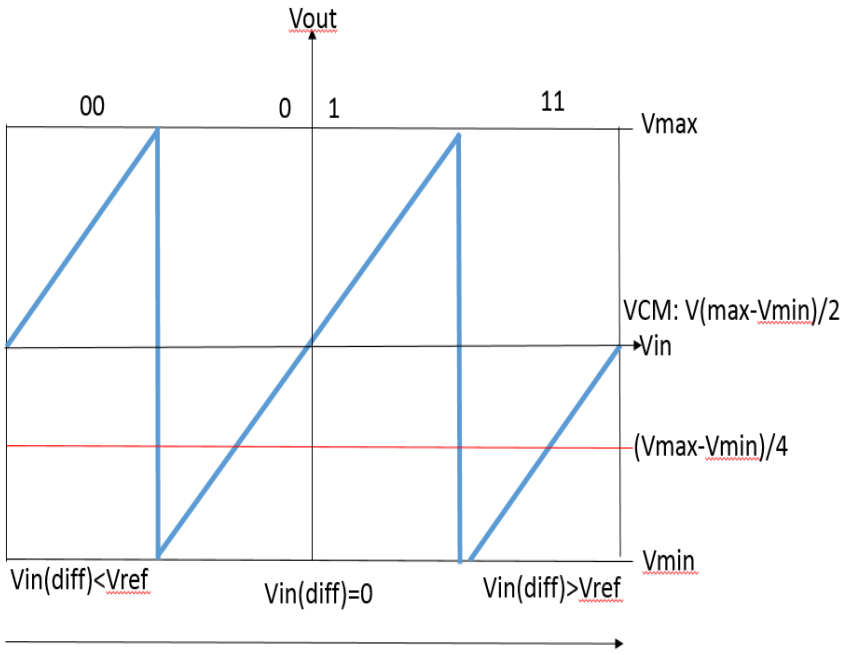

Figure 2.14 1.5 bits transfer curve

Since it is for differential signaling, 2 separate comparators are needed to do comparison for each signal, the Vref is defined as

$$Vrefmin: Vmin + \frac{(VCM - Vmin)}{2} \tag{2.4}$$

3 separate zones can be defined.

1. Zone -1 (00) : $Vin_{diff} < Vref$
2. Zone 0 (01) : $Vrefmin < Vin_{diff} < Vrefmax$

3. Zone 1 (11): $Vrefmax < Vin_{diff}$

The output of the comparator will be a 2 bits output to decode 3 different zones. The output be used as inputs to determine the voltage that the residue amplifier will need to substrate to. The speed of the comparator is very important and must be settled within the Ph1 during sampling time else it will pass the wrong into to decoder. There are few ways to form the comparator, the most common architecture is the op amp based comparator. The speed is fast and can operate at frequency of up to 1 Ghz. The disadvantages is the power needed for generating the current source and the bias voltage for the op amp. The other common architecture is sense amp latch. It is a clock gated latch with will perform in differential mode as well. The power consumption is much lesser because it is enabled by a gated clock but the performance is lower as compare to op amp. Figure 2.15 and Figure 2.16 below is showing how to apply the op-amp and sense amp for the comparator.

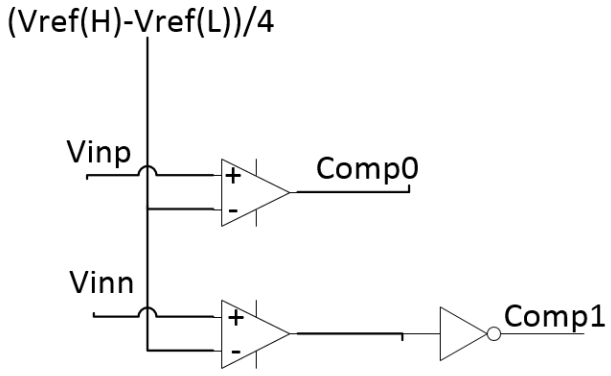

Figure 2.15 Op amp as comparator

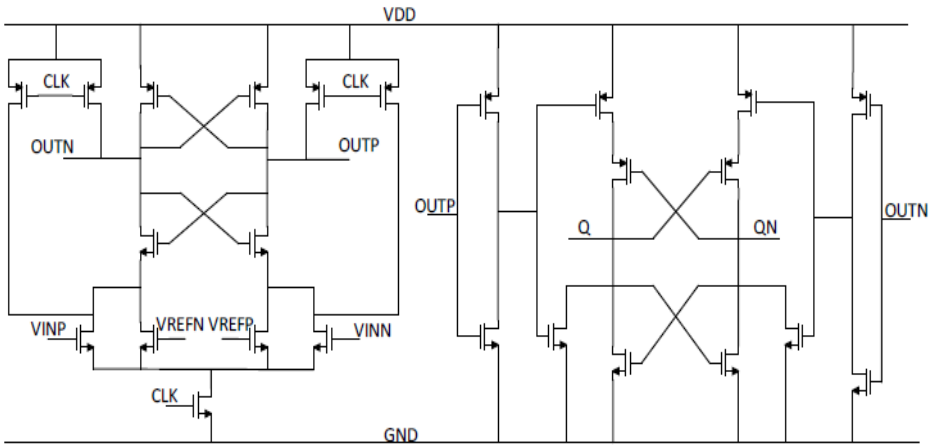

Figure 2.16 Sense amp latch as comparator (Teng Chen et al., 2015)

2.3.2.3 Decoder and analog multiplexer

The purpose of the decoder is to decode the two input signals and output the dedicated voltage to the residue amplifier during amplification time. Based on the MDAC configuration in Figure 2.5 above, the simplified structure of Mux circuit and mapping is as Figure 2.17 below